# EXPLORATION OF RING OSCILLATOR DESIGN SPACE FOR TEMPERATURE MEASUREMENTS ON FPGAS

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## ABSTRACT

While numerous publications have presented ring oscillator designs for temperature measurements a detailed study of the ring oscillator's design space is still missing. In this work, we introduce metrics for comparing the performance and area efficiency of ring oscillators and a methodology for determining these metrics. As a result, we present a systematic study of the design space for ring oscillators for a Xilinx Virtex-5 platform FPGA.

## 1. INTRODUCTION

With shrinking device structures and increasing device densities, thermal effects gain more and more importance in the domain of FPGA-based systems. For traditional VLSI systems the designer has to account for thermal effects during design time while reconfigurable systems allow for a response to temperature effects during runtime, through reconfiguration.

Several approaches that deal with thermal issues on FPGAs rely on knowing the current on-chip temperature distribution. For multi-processor systems there exist reactive techniques—such as dynamic voltage and frequency scaling —and proactive techniques—such as task migration, i.e. [1]. While there are methods that allow for obtaining accurate and fine-grained temperature distributions, they rely on external devices, i.e. infrared cameras [2], that are expensive and cannot be employed in the field.

Thus, many researchers employ ring oscillators (ROs) as temperature sensors on FPGAs [2, 3, 4]. Research on RO-based temperature sensors includes sensor placement [5], sensor calibration [6, 7] and workload effects on the measurement performance [8]. While numerous publications have presented RO designs for temperature measurements, a detailed study of the RO design space is still missing.

In this paper, we introduce metrics for comparing the performance and area efficiency of ROs and a methodology for the experimental evaluation of a broad range of sensor designs. We target modern Xilinx FPGAs that contain a pre-calibrated built-in thermal diode, which we use for calibration and evaluation purposes. The examined designs differ in the RO size, slice utilization and in routing. We evaluate noise and measurement accuracy of the sensors and investigate the influence of a number of design parameters. This paper makes the following contributions:

- A detailed study of the design space of RO-based temperature sensors on modern FPGAs.
- A methodology to evaluate the performance of the temperature sensors.
- Comprehensive experimental results on designing temperature sensors on a Xilinx Virtex-5 FPGA.

Section 2 gives an overview on related work. In Section 3 we describe the design parameters of our temperature sensors and propose an evaluation methodology. Section 4 presents our experimental results. Finally, Section 5 concludes the paper.

## 2. RELATED WORK

ROs are widely used as temperature sensors in FPGA-based systems. For instance, Lopez-Buedo et al. [6] showed that the frequency of a RO is inversely proportional to the temperature. Their sensor consists of a RO with 7 inverters, a timebase counter and a capture counter. In [6, 3] the sensors were calibrated using a temperature-controlled oven.

In our previous work [7] we proposed self-calibrating temperature sensors based on ROs. The system contains an array of temperature sensors and calibrates them using an internal pre-calibrated thermal diode and internal regional heat-generating cores on a Virtex-6 FPGA.

Sayed and Jones [8] characterized the impacts of reconfigurable hardware workload on ROs on Xilinx Virtex-5 FPGAs. Recently, Zick and Hayes [4] proposed a low cost RO-based sensor to measure not only temperature but also delay, leakage and dynamic power on a Xilinx Virtex-5 FPGA.

Similar to [6, 7, 8] we use a RO combined with a timebase counter and a capture counter as temperature sensor. Furthermore, we access the temperature readings of our sen-

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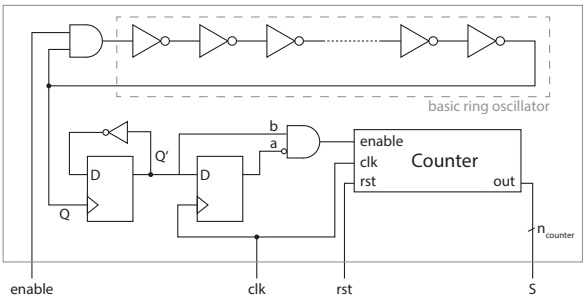


**Fig. 1**. Simplified schematic of our temperature sensor

sors using a daisy chain as proposed in [4]. In contrast to related work, we did an exhaustive study to evaluate the influence of different parameters—such as the measurement period, number of inverters and use of latches—on the measurement performance of RO-based temperature sensors.

## 3. PARAMETERS AND METHODOLOGY

A RO circuit is composed of an odd number of inverters as shown in Figure 1. Its output $Q$ oscillates between 0 and 1 at a frequency $f$ based on the circuit's delay. For a given sensor implementation, this delay depends on the operating voltage and temperature. Assuming constant operating voltage, an increase in temperature leads to an increased delay and thus a decrease in $f$. To design a temperature sensor we extended the basic RO as shown in Figure 1. A measurement includes the following steps:

- Enable the ring oscillator.
- Wait $2^{12}$ clock cycles so that the RO can gain a constant frequency.
- Sample $Q'$ for $t_m$ clock cycles and disable the RO.
- Read out the counter value $S$.

In the design of the temperature sensor there are a number of parameters that need to be concretized for implementation. The *measurement period* $t_m$ is the time interval during which we sample the RO output signal. While a longer $t_m$ should lead to more accurate results, issues like self-heating, area allocated to the oscillation counter and the ability to obtain a time series of sensor readings with high temporal resolution, constrain the measurement period. The *number of inverters* and other delay elements such as *latches* have a significant effect on the performance of the RO. And finally, the placement of the RO elements, as well as routing have an impact on the sensor's performance.

### 3.1. Evaluation

To test our sensors we need an independent way to determine the on-chip temperature. For this, we use the built-in system monitor of the FPGA that uses a thermal diode with an accuracy of $\pm 4°$C as specified by the manufacturer [9].

For our evaluation of the different sensor designs, we establish an evaluation function that takes into account the sensor resolution $\sigma_v$ and the sensor noise, expressed as the standard deviation $\sigma_c$ of the sensor readings. We calculate the resolution of the sensor as

$$\sigma_v := \frac{S_{max} - S_{min}}{T_{max} - T_{min}} \tag{1}$$

where $S_{max}$ and $S_{min}$ are the number of oscillations measured in the time interval $t_m$ at maximum and minimum temperatures $T_{max}$ and $T_{min}$, respectively. This value indicates how much the sensor count changes at a given temperature difference.

Sensor noise is determined over a time series of $n$ single measurements at constant temperature with sensor readouts $S_i$ and an average of $\overline{S}$.

$$\sigma_c := \sqrt{\frac{1}{n}\sum_{i=1}^{n}(S_i - \overline{S})^2} \tag{2}$$

Since we expect a quantization noise of $\sigma = 0.5$ the value $\sigma_c$ is clamped at $0.5$ for low-noise sensors that happen to encounter little quantization error.

We can then calculate the performance $G$ of the sensor

$$G := \frac{\sigma_v}{\sigma_c} \tag{3}$$

which can be seen as the sensor's signal to noise ratio and gives us a good indication of how well the sensor balances noise versus resolution.

### 3.2. Calibration

Because of variations in the manufacturing process, operating voltage, sensor routing, etc., it is not possible, in practice to predict the function that maps sensor count $S$ to a temperature $T$. We therefore need to calibrate the individual sensors. As demonstrated in [6], a linear mapping from $S$ to $T$ gives us a very good approximation. In order to calibrate the sensors, we heat up and cool down the FPGA while reading out the sensor counts and the temperature values provided by the built-in system monitor in regular time intervals. We then determine for each sensor the mapping function from $S$ to $T$ by partial regression.

## 4. EXPERIMENTAL RESULTS

In this section we introduce our experimental setup, describe the experiments that have been performed for evaluating the RO design space and discuss our results.

### 4.1. System setup

Our system setup consists of three major components. The Xilinx XUPV5 board which features a Xilinx XC5VLX110T FPGA, an external electromechanical heating device, and a PC connected via UART to the FPGA, which is used to log sensor and system monitor readings and to control the heat source. To monitor the core voltage and the thermal readings

provided by the built-in diode, we use the system monitor core supplied by Xilinx.

The sensors are synthesized from a VHDL specification that makes use of device-specific primitives to directly instantiate inverters and enable-logic. In addition to the VHDL description, the RO's components are placed using placement directives in the UCF-File. This allows us to pin down individual LUTs and latches to specific slices on the FPGA. The routing is done automatically using vendor tools which employ a randomized algorithm that may produce different results each time a sensor is routed. While this greatly simplifies the task of evaluating a huge number of sensors with different design parameters, the variations in routing have to be accounted for. We did so by evaluating each sensor design by placing 16 instances of the sensor in a regular 4x4 grid on the FPGA. We then averaged the resulting values for sensor performance $G$ in order to decrease the impacts of routing variations.

### 4.2. Experiments

To evaluate the noise and resolution, we performed two tests for each sensor design. The first test serves to measure the sensor's noise by taking a series of sensor measurements for ten seconds, while keeping the FPGA at a constant temperature. The second test is used to determine the sensor's resolution by heating up the chip an letting it cool down two times over a period of 780 seconds.

We examined a wide array of possible RO designs based on the variation of a number of design parameters. We examined the effect of the measurement period on sensor noise as well as the influence of sensor size (number of LUTs) and the use of latches on the sensor's performance.

**Measurement period:** In order to determine the effect of the measurement period $t_m$, we measured the noise of sensors of different sizes over varying values for $t_m$. Figure 2 shows the noise as a percentage of the average oscillation count for different measurement periods expressed in clock cycles of a 100MHz clock. It can be seen that the noise decreases with an increase of $t_m$ from $2^{13}$ to $2^{16}$ clock cycles. This is mostly due to quantization noise which we expect to be at least $0.012\%$ for $t_m = 2^{13}$ clock cycles. A further increase of $t_m$, however, does not result in a lower noise, as other sources of noise come into play. Therefore, to minimize the impact of self heating, and to save reconfigurable resources that have to be allocated to the oscillation counter, we conclude that with respect to sensor noise, a measurement period of more than $2^{16}$ clock cycles ($655\mu$s) is not advisable.

**Number of inverters:** In order to examine the influence of the RO's size we examined several design combinations and evaluated their respective sensor performance. First, we experimented with variations in the number of LUT-based inverter elements. Table 1 shows for each sensor design the values of $\sigma_c$ and $\sigma_v$ in units of oscillations per measurement. It shows that, while noise decreases with the number of inverters, eventually approaching the level of quantization noise, the resolution also decreases, giving rise to a broad optimum in sensor performance at 47 inverters.

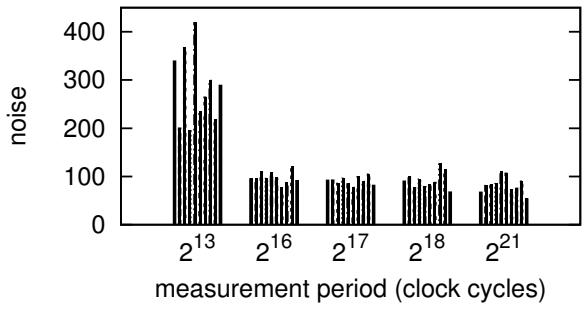


**Fig. 2**. Noise (measured in parts per million) for different sensor sizes and measurement periods.

**Use of latches:** As suggested in [4], slice latches that are held in the open state can be built into the oscillator circuit. An advantage of this is, that the latches are basically free resources, since on the FPGA each LUT has an associated latch/flip-flop component that can be connected to the LUT's output without the use of additional routing resources.

For our evaluation, we used the sensor with 47 inverter elements since according to Table 1 this is the best performing candidate. We then replaced some of the inverters with

**Table 1**. Average oscillation count, sensor noise, resolution and performance for different numbers of inverters

| # Inverter | $\bar{S}$ at 46°C | $\sigma_c$ | $\sigma_v$ | $G$ |
|---|---|---|---|---|
| 17 | 24913 | 2.4342 | 17.6854 | 7.2654 |
| 23 | 18913 | 1.6990 | 13.4893 | 7.9395 |
| 31 | 16263 | 1.4622 | 12.1500 | 8.3092 |
| 47 | 11495 | 1.0524 | 8.8124 | 8.3737 |
| 63 | 8817 | 0.8218 | 6.8201 | 8.2988 |
| 79 | 6956 | 0.6862 | 5.4568 | 7.9526 |
| 95 | 5889 | 0.5906 | 4.5791 | 7.7540 |
| 111 | 5038 | 0.5200 | 3.8920 | 7.4841 |

**Table 2**. Sensor noise, resolution and performance for different combinations of LUTs and latches.

| # Latches | # Inverters | $\sigma_c$ | $\sigma_v$ | $G$ |
|---|---|---|---|---|
| 0 | 47 | 1.0524 | 8.8124 | 8.3737 |
| 16 | 31 | 0.9078 | 7.4713 | 8.2302 |
| 24 | 23 | 0.8459 | 7.9499 | 9.3977 |
| 32 | 15 | 0.7668 | 6.9368 | 9.0465 |
| 38 | 9 | 0.7961 | 6.9750 | 8.7611 |
| 42 | 5 | 0.7993 | 6.7145 | 8.4001 |
| 46 | 1 | 0.8270 | 6.7962 | 8.2180 |

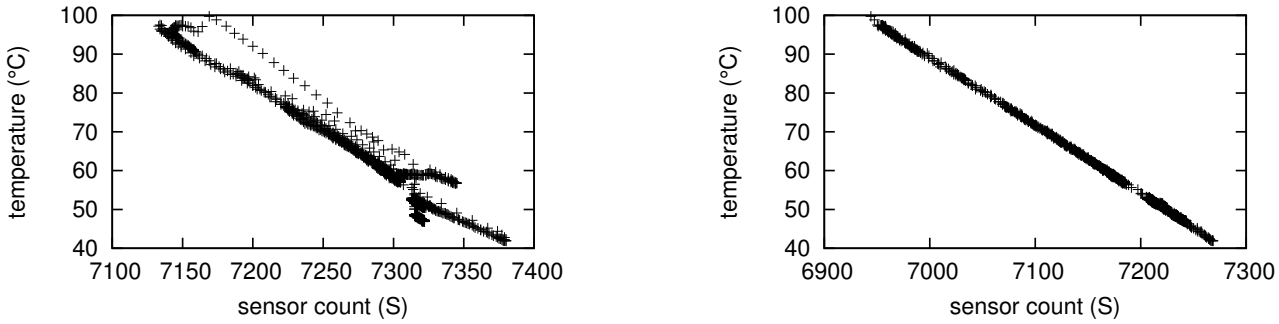


**Fig. 3**. Exemplary sensor measurements. Left: Without voltage correction, right: After correcting for voltage variations.

latches and tested the sensor again using the procedure described above. As can be seen in Table 1, we were able to improve the performance of the sensor by up to 13.8% using 24 latches and 23 inverters.

### 4.3. Compensation of voltage fluctuations

While conducting our experiments, we noticed that the relation between the temperature reported by the system monitor and the oscillation frequencies of our sensors differed between the heat up and cool down periods. Also, there was a variation in core voltage as reported by the system monitor.

Further investigation revealed that the differences in system monitor temperature with respect to the sensor readings are proportional to the core voltage changes. While we can only speculate about the source of the voltage variations, the dependency of a RO's frequency on operating voltage is well known and documented. In order to correct the sensor readings for voltage fluctuations, we calculate a corrected oscillation count $S' = S + aV$ from the raw sensor readout $S$ and the voltage $V$ as reported by the system monitor.

In order to obtain the coefficient $a$ we take advantage of the linear relationship between the temperature and the RO frequency and choose $a$ in such a manner that this relationship is optimally satisfied.

Figure 3(a) shows a set of measurements without correction. Each point represents a raw sensor reading (oscillation count) with the associated system monitor temperature reading. The sample points should lie on a line, but instead produce curves with different slopes depending on the direction of the temperature changes. Figure 3(b) shows the same sample set after the correction is applied.

## 5. CONCLUSION

In this paper, we defined design parameters of temperature sensors, that are based on ring oscillators, and proposed a method to evaluate the overall sensor performance based on sensor noise and resolution. As design parameters, we examined the measurement period, the ring oscillator size and the use of different delay elements. We performed an extensive design space exploration on a Xilinx Virtex-5 FPGA. Our experimental results show that the measurement period should not be longer than 655$\mu$s. Furthermore, the ring oscillator comprising 23 inverters and 24 latches gives the best overall performance according to our evaluation criteria. Finally, we could increase the reliability of the sensor measurements by correcting for voltage variations.

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